IFW

PATENT

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January 9, 2006 — Date

Denise Sheridan — Denise Sheridan

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/629,156	Confirmation No.	: 5983
Applicant	: Graham Kirsch		
Filed	: July 28, 2003	Attorney Docket No.	: 501276.02
Art Unit	: 2187	Customer No.	: 27,076
Examiner	: Nasser G. Moazzami		
Title	: SYSTEM AND METHOD FOR ENCODING PROCESSING ELEMENT COMMANDS IN AN ACTIVE MEMORY DEVICE		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37 C.F.R. § 1.111

Sir:

Applicant acknowledges receipt of the Office Action dated November 14, 2005. Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 20 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1, 6, 9, 16, 30, 35, 38, 45 and 49 as follows:

Listing of Claims:

1. (Currently Amended) An integrated circuit active memory device comprising:

a command engine operable to generate either respective sequences of array control unit commands or respective sequences of memory device control unit commands responsive to respective task commands applied to a task command input of the command engine;

an array control unit coupled to receive the sequences of the array control unit commands from the command engine, the array control unit being operable to generate a respective sequence of processing element instructions responsive to each of the sequences of the array control unit commands;

a memory device control unit coupled to receive the sequences of the memory device control unit commands from the command engine, the memory device control unit being operable to generate a respective sequence of memory commands responsive to each of the sequences of the memory device control unit commands;

a decode memory device coupled to receive the sequences of the processing element instructions from the array control unit, the decode memory device storing a plurality of processing element microinstructions and being addressed by the sequences of the processing element instructions such that each of the processing element instructions accesses a location in the decode memory device where a respective processing element microinstruction is stored, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the processing element instructions;

a memory device having a data bus containing a plurality of data bus bits, the memory device being operable to receive the memory device control unit commands and couple write data to and read data from the memory device through the data bus; and

an array of processing elements each of which is coupled to a respective group of the data bus bits of the memory device data bus, each of the processing elements having an instruction input coupled to receive the plurality of the processing element microinstructions from the decode memory device for controlling the operation of the processing elements.

2. (Original) The active memory device of claim 1 wherein the memory device comprises a random access memory device.

3. (Original) The active memory device of claim 2, wherein the decode memory device comprises a static random access memory device.

4. (Original) The active memory device of claim 1, further comprising:

a plurality of instruction registers coupled to receive the processing element instructions from the array control unit, the instruction registers being operable to store a plurality of the processing element instructions and to simultaneously output the processing element instructions stored in the instruction registers as a processing element microinstruction; and

a multiplexer having a first input coupled to the output port of the decode memory device to receive the processing element microinstructions from the decode memory device, a second input coupled to the instruction registers to receive the processing element micro instructions output from the instruction registers, and an output coupled to the instruction input of each of the processing elements.

5. (Original) The active memory device of claim 1 wherein the array control unit is further operable to generate an array control unit instruction along with each of the

processing element instructions, the array control unit instruction controlling the operation of the array control unit.

6. (Currently Amended) The active memory device of claim 1 wherein the array control unit further comprises:

a program cache device containing a plurality of array control unit instructions, at least some of the array control unit instructions including an array control unit microinstruction and one of the processing element instructions, the array control unit microinstructions being passed to the array control unit to control the operation of the array control unit; and

a cache control device that is operable to address the program cache device responsive to control signals from the array control unit, at least some of the control signals being responsive to the sequences of the array control unit commands to cause the cache control device to access a specific location in the cache control device where an array control instruction is stored.

7. (Original) The active memory device of claim 6, further comprising a program port coupled to the program cache device, the program port receiving the array control unit instructions, and coupling the array control unit instructions to the program cache device to program the program cache device prior to operation of the array control unit.

8. (Original) The active memory device of claim 1, further comprising a program port coupled to the decode memory device, the program port receiving the processing element microinstructions and coupling the processing element microinstruction to the decode memory device to program the decode memory device prior to operation of the array control unit.

9. (Currently Amended) An integrated circuit active memory device comprising:

a command engine operable to generate either respective sequences of array control unit commands or respective sequences of memory device control unit commands responsive to respective task commands applied to a task command input of the command engine;

an array control unit coupled to receive the sequences of the array control unit commands from the command engine, the array control unit comprising:

a program cache device containing a plurality of array control unit instructions, at least some of the array control unit instructions including an array control unit microinstruction and a processing element instruction, the array control unit microinstructions being passed to the array control unit to control the operation of the array control unit; and

a cache control device that is operable to address the program cache device responsive to control signals from the array control unit, at least some of the control signals being responsive to the sequences of the array control unit commands to cause the cache control device to access a specific location in the cache control device where an array control instruction is stored;

a memory device control unit coupled to receive the sequences of the memory device control unit commands from the command engine, the memory device control unit being operable to generate a respective sequence of memory commands responsive to each of the sequences of the memory device control unit commands;

a decode memory device coupled to receive the processing element instructions from the program cache, the decode memory device storing a plurality of processing element microinstructions and being addressed by the processing element instructions such that each of the processing element instructions accesses a location in the decode memory device where a respective processing element microinstruction is stored, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the processing element instructions;

a memory device having a data bus containing a plurality of data bus bits, the memory device being operable to receive the sequences of the memory commands and couple write data to and read data from the memory device through the data bus; and

an array of processing elements each of which is coupled to a respective group of the data bus bits of the memory device data bus, each of the processing elements having an instruction input coupled to receive the processing element microinstructions from the decode memory for controlling the operation of the processing elements.

10. (Original) The active memory device of claim 9, further comprising a program port coupled to the decode memory device, the program port receiving the processing element microinstructions and coupling the processing element microinstruction to the decode memory device to program the decode memory device prior to operation of the array control unit.

11. (Original) The active memory device of claim 9, further comprising a program port coupled to the program cache device, the program port receiving the processing element instructions and coupling the processing element instruction to the program cache device to program the program cache device prior to operation of the array control unit.

12. (Original) The active memory device of claim 9, further comprising a program port coupled to the program cache device and to the decode memory device, the program port receiving the processing element instructions and coupling the processing element instruction to the program cache device for storage in the program cache device prior to operation of the array control unit, the program port further receiving the processing element microinstructions and coupling the processing element microinstruction to the decode memory device for storage in the decode memory device prior to operation of the array control unit, the processing element microinstructions stored in the decode memory corresponding to the processing element instructions stored in the program cache device.

13. (Original) The active memory device of claim 9 wherein the decode memory device comprises a random access memory device.

14. (Original) The active memory device of claim 13 wherein the decode memory device comprises a static random access memory device.

15. (Original) The active memory device of claim 9, further comprising:

a plurality of instruction registers coupled to receive the processing element instructions from the array control unit, the instruction registers being operable to store at least a portion of each of a plurality of the processing element instructions and to simultaneously output the stored portions of the processing element instructions as a processing element microinstruction; and

a multiplexer having a first input coupled to the output port of the decode memory device to receive the processing element microinstructions from the decode memory device, a second input coupled to the instruction registers to receive the processing element micro instructions output from the instruction registers, and an output coupled to the instruction input of each of the processing elements.

16. (Currently Amended) An integrated circuit single instruction multiple data processing device, comprising:

a command engine operable to generate respective sequences of array control unit commands responsive to respective task commands applied to a task command input of the command engine;

an array control unit coupled to receive the sequences of the array control unit commands from the command engine, the array control unit comprising:

a program cache device containing a plurality of array control unit instructions, at least some of the array control unit instructions including an array control unit microinstruction and a processing element instruction, the array control unit

microinstructions being passed to the array control unit to control the operation of the array control unit; and

a cache control device that is operable to address the program cache device responsive to control signals from the array control unit, at least some of the control signals being responsive to the sequences of the array control unit commands to cause the cache control device to access a specific location in the cache control device where an array control instruction is stored;

a decode memory device coupled to receive the processing element instructions from the program cache, the decode memory device storing a plurality of processing element microinstructions and being addressed by the processing element instructions such that each of the processing element instructions accesses a location in the decode memory device where a respective processing element microinstruction is stored, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the processing element instructions; and

an array of processing elements each of which is coupled to a respective group of the data bus bits of the memory device data bus, each of the processing elements having an instruction input coupled to receive the processing element microinstructions from the decode memory for controlling the operation of the processing elements.

17. (Original) The processing device of claim 16, further comprising a program port coupled to the decode memory device, the program port receiving the processing element microinstructions and coupling the processing element microinstruction to the decode memory device to program the decode memory device prior to operation of the array control unit.

18. (Original) The processing device of claim 16, further comprising a program port coupled to the program cache device, the program port receiving the processing element instructions and coupling the processing element instruction to the program cache device to program the program cache device prior to operation of the array control unit.

19. (Original) The processing device of claim 16, further comprising a program port coupled to the program cache device and to the decode memory device, the program port receiving the processing element instructions and coupling the processing element instruction to the program cache device for storage in the program cache device prior to operation of the array control unit, the program port further receiving the processing element microinstructions and coupling the processing element microinstruction to the decode memory device for storage in the decode memory device prior to operation of the array control unit, the processing element microinstructions stored in the decode memory corresponding to the processing element instructions stored in the program cache device.

20. (Original) The processing device of claim 16 wherein the decode memory device comprises a random access memory device.

21. (Original) The processing device of claim 20 wherein the decode memory device comprises a static random access memory device.

22. (Original) The processing device of claim 16, further comprising:

a plurality of instruction registers coupled to receive the processing element instructions from the array control unit, the instruction registers being operable to store at least a portion of each of a plurality of the processing element instructions and to simultaneously output the stored portions of the processing element instructions as a processing element microinstruction; and

a multiplexer having a first input coupled to the output port of the decode memory device to receive the processing element microinstructions from the decode memory device, a second input coupled to the instruction registers to receive the processing element micro instructions output from the instruction registers, and an output coupled to the instruction input of each of the processing elements.

23. (Original) An active memory control system, comprising:

a first control device receiving task commands corresponding to respective active memory operations, the first control device being operable to generate either a respective set of memory commands or a respective set of processing commands responsive to each of the task commands;

a second control device coupled to receive the memory commands from the first control device, the second control device being operable to generate a respective set of the memory device instructions responsive to each of the memory commands;

a third control device coupled to receive the processing commands from the first control device, the third control device being operable to generate a respective set of the processing element instructions responsive to each of the processing commands.

a decode memory device coupled to receive the processing element instructions from the third control device, the decode memory device storing a plurality of processing element microinstructions and being addressed by the processing element instructions such that each of the processing element instructions accesses a location in the decode memory device where a respective processing element microinstruction is stored, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the processing element instructions.

24. (Original) The active memory control system of claim 23, wherein the decode memory device comprises a random access memory device.

25. (Original) The active memory control system of claim 24, wherein the decode memory device comprises a static random access memory device.

26. (Original) The active memory control system of claim 23, further comprising:

a plurality of instruction registers coupled to receive the processing element instructions from the third control device, the instruction registers being operable to store a plurality of the processing element instructions and to simultaneously output the processing

element instructions stored in the instruction registers as a processing element microinstruction; and

a multiplexer having a first input coupled to the output port of the decode memory device to receive the processing element microinstructions from the decode memory device, a second input coupled to the instruction registers to receive the processing element micro instructions output from the instruction registers, the multiplexer being operable to couple either the first input or the second input to an output.

27. (Original) The active memory control system of claim 23 wherein the third control device is further operable to generate a control instruction along with each of the processing element instructions, the control instruction controlling the operation of the third control device.

28. (Original) The active memory control system of claim 23 wherein the third control device further comprises:

a program cache device containing a plurality of instructions, at least some of the instructions including a control unit microinstruction and one of the processing element instructions, the control unit microinstructions being passed to the third control device to control the operation of the array control unit; and

a cache control device that is operable to address the program cache device responsive to control signals from the third control device, at least some of the control signals being responsive to the control unit microinstruction to cause the cache control device to access a specific location in the cache control device where one of the instructions is stored.

29. (Original) The active memory control system of claim 28, further comprising a program port coupled to the program cache device, the program port receiving the instructions, and coupling the instructions to the program cache device to program the program cache device prior to operation of the third control device.

30. (Currently Amended) A computer system, comprising:

a host processor having a processor bus;

at least one input device coupled to the host processor through the processor bus;

at least one output device coupled to the host processor through the processor bus;

at least data storage device coupled to the host processor through the processor bus; and

an active memory device, comprising:

a command engine operable to generate either respective sequences of array control unit commands or respective sequences of memory device control unit commands responsive to respective task commands applied to a task command input of the command engine;

an array control unit coupled to receive the sequences of the array control unit commands from the command engine, the array control unit being operable to generate a respective sequence of processing element instructions responsive to each of the sequences of the array control unit commands;

a memory device control unit coupled to receive the sequences of the memory device control unit commands from the command engine, the memory device control unit being operable to generate a respective sequence of memory commands responsive to each of the sequences of the memory device control unit commands;

a decode memory device coupled to receive the processing element instructions from the array control unit, the decode memory device storing a plurality of processing element microinstructions and being addressed by the processing element instructions such that each of the processing element instructions accesses a location in the decode memory device where a respective processing element microinstruction is stored, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the processing element instructions;

a memory device having a data bus containing a plurality of data bus bits, the memory device being operable to receive the sequences of the memory commands and couple write data to and read data from the memory device through the data bus; and

an array of processing elements each of which is coupled to a respective group of the data bus bits of the memory device data bus, each of the processing elements having an instruction input coupled to receive the processing element microinstructions from the decode memory for controlling the operation of the processing elements.

31. (Original) The computer system of claim 30 wherein the memory device comprises a random access memory device.

32. (Original) The computer system of claim 31, wherein the decode memory device comprises a static random access memory device.

33. (Original) The computer system of claim 30, further comprising:

a plurality of instruction registers coupled to receive the processing element instructions from the array control unit, the instruction registers being operable to store a plurality of the processing element instructions and to simultaneously output the processing element instructions stored in the instruction registers as a processing element microinstruction; and

a multiplexer having a first input coupled to the output port of the decode memory device to receive the processing element microinstructions from the decode memory device, a second input coupled to the instruction registers to receive the processing element micro instructions output from the instruction registers, and an output coupled to the instruction input of each of the processing elements.

34. (Original) The computer system of claim 30 wherein the array control unit is further operable to generate an array control unit instruction along with each of the processing element instructions, the array control unit instruction controlling the operation of the array control unit.

35. (Currently Amended) The computer system of claim 30 wherein the array control unit further comprises:

a program cache device containing a plurality of array control unit instructions, at least some of the array control unit instructions including an array control unit microinstruction and one of the processing element instructions, the array control unit microinstructions being passed to the array control unit to control the operation of the array control unit; and

a cache control device that is operable to address the program cache device responsive to control signals from the array control unit, at least some of the control signals being responsive to the sequences of the array control unit commands to cause the cache control device to access a specific location in the cache control device where an array control instruction is stored.

36. (Original) The computer system of claim 35, further comprising a program port coupled to the program cache device, the program port receiving the array control unit instructions, and coupling the array control unit instructions to the program cache device to program the program cache device prior to operation of the array control unit.

37. (Original) The computer system of claim 30, further comprising a program port coupled to the decode memory device, the program port receiving the processing element microinstructions and coupling the processing element microinstruction to the decode memory device to program the decode memory device prior to operation of the array control unit.

38. (Currently Amended) A computer system, comprising:

a host processor having a processor bus;

at least one input device coupled to the host processor through the processor bus;

at least one output device coupled to the host processor through the processor bus;

at least data storage device coupled to the host processor through the processor bus; and

an active memory device, comprising:

a first control device receiving task commands from the host processor corresponding to respective active memory operations, the first control device being operable to generate either a respective set of memory commands or a respective set of processing commands responsive to each of the task commands;

a second control device coupled to receive the sets of the memory commands from the first control device, the second control device being operable to generate a respective set of the memory device instructions responsive to each of the sets of the memory commands;

a third control device coupled to receive the sets of the processing commands from the first control device, the third control device being operable to generate a respective set of the processing element instructions responsive to each of the sets of the processing commands;

a decode memory device coupled to receive the processing element instructions from the third control device, the decode memory device storing a plurality of processing element microinstructions and being addressed by the processing element instructions such that each of the processing element instructions accesses a location in the decode memory device where a respective processing element microinstruction is stored, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the processing element instructions;

a memory device having a data bus containing a plurality of data bus bits, the memory device being coupled to second control device to receive the memory device instructions and couple write data to and read data from the memory device through the data bus responsive to the memory device instructions; and

an array of processing elements each of which is coupled a respective group of the data bus bits of the memory device data bus, each of the processing elements having an instruction input coupled to the third control device to receive the processing element microinstructions for controlling the operation of the processing elements.

39. (Original) The computer system of claim 38, wherein the decode memory device comprises a random access memory device.

40. (Original) The computer system device of claim 39, wherein the decode memory device comprises a static random access memory device.

41. (Original) The computer system device of claim 38, further comprising:

a plurality of instruction registers coupled to receive the processing element instructions from the third control device, the instruction registers being operable to store a plurality of the processing element instructions and to simultaneously output the processing element instructions stored in the instruction registers as a processing element microinstruction; and

a multiplexer having a first input coupled to the output port of the decode memory device to receive the processing element microinstructions from the decode memory device, a second input coupled to the instruction registers to receive the processing element micro instructions output from the instruction registers, the multiplexer being operable to couple either the first input or the second input to an output.

42. (Original) The computer system of claim 38 wherein the third control device is further operable to generate a control instruction along with each of the processing element instructions, the control instruction controlling the operation of the third control device.

43. (Original) The computer system of claim 38 wherein the third control device further comprises:

a program cache device containing a plurality of instructions, at least some of the instructions including a control unit microinstruction and one of the processing element instructions, the control unit microinstructions being passed to the third control device to control the operation of the array control unit; and

a cache control device that is operable to address the program cache device responsive to control signals from the third control device, at least some of the control signals being responsive to the control unit microinstruction to cause the cache control device to access a specific location in the cache control device where one of the instructions is stored.

44. (Original) The computer system of claim 43, further comprising a program port coupled to the program cache device, the program port receiving the instructions, and coupling the instructions to the program cache device to program the program cache device prior to operation of the third control device.

45. (Currently Amended) A method of controlling the operation of a memory device and an array of processing elements that are coupled to the memory device, the method comprising:

receiving a task command corresponding to an active memory operation;

generating either a set of array commands or a set of memory device commands responsive to the task command;

generating a respective set of processing element instructions responsive to each of the sets of the array commands;

generating a respective set of memory device instructions responsive to each of the sets of the memory device commands;

selecting a processing element microinstruction responsive to each of the processing element instructions, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the corresponding processing element instructions;

controlling the memory device responsive to the memory device instructions; and

controlling the processing elements in the array responsive to the processing element microinstructions.

46. (Original) The method of claim 45 wherein at least some of the processing element instructions comprise respective storage device addresses, and wherein the act of selecting a processing element microinstruction comprises:

storing the processing element microinstructions at respective addresses in a storage device; and

using the processing element instructions to address the storage device.

47. (Original) The method of claim 46 wherein the act of storing the processing element microinstructions comprises storing the processing element microinstructions in the storage device prior to operation of the a memory device and processing elements based on the operations that are to be performed by the memory device or processing elements.

48. (Original) The method of claim 46, further comprising combining at least portions of a plurality of the processing element instructions and simultaneously outputting the combined processing element instructions as an extra length one of the processing element microinstructions.

49. (Currently Amended) A method of processing data, comprising:

receiving a task command corresponding to a processing operation;

generating a set of processing commands responsive to the task command;

generating a respective set of processing element instructions responsive to each of the sets of the processing commands;

selecting a processing element microinstruction responsive to each of the processing element instructions, each of the processing element microinstructions having a number of bits that is greater than the number of bits in the corresponding processing element instructions; and

processing the data responsive to the processing element microinstructions.

50. (Original) The method of claim 49 wherein at least some of the processing element instructions comprise respective storage device addresses, and wherein the act of selecting a processing element microinstruction comprises:

storing the processing element microinstructions at respective addresses in a storage device; and

using the processing element instructions to address the storage device.

51. (Original) The method of claim 49 wherein the act of storing the processing element microinstructions comprises storing the processing element microinstructions in the storage device prior to operation of the processing elements based on the operations that are to be performed by the processing elements.

52. (Original) The method of claim 49, further comprising combining at least portions of a plurality of the processing element instructions and simultaneously outputting the combined processing element instructions as an extra length one of the processing element microinstructions.

REMARKS

Claims 1-52 are pending in this application. In the Office Action dated November 14, 2005, the Examiner objected to claims 1-52 for informalities but would otherwise be allowed if rewritten to overcome the informalities.

Applicant notes that this application is in condition for allowance except for the claim informalities and that prosecution as to the merits has been closed in accordance with the practice under *Ex parte Quayle.* Applicant has amended the claims to overcome the claim objections.

All of the claims in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are therefore earnestly solicited.

Respectfully submitted,

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EWB:dms

Enclosures:
Postcard
Fee Transmittal Sheet (+copy)

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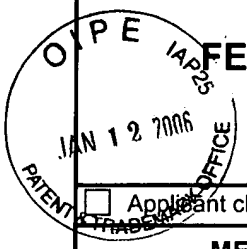
Effective on 12/08/04



FEE TRANSMITTAL SHEET (FY 2005)

Complete if Known	
Application No.	10/629,156
Filing Date	July 28, 2003
First Inventor	Graham Kirsch
Group Art Unit	2187
Examiner Name	Nasser G. Moazzami
Atty. Docket Number	501276.02

☐ Applicant claims small entity status (see 37 C.F.R. 1.27)

METHOD OF PAYMENT (Check One)

☒ The Director is hereby authorized to charge any additional fee required under 37 C.F.R. §§ 1.16 and 1.17 and 1.136(a)(3) and credit any over payments to Deposit Account No. **50-1266;** Deposit Account Name: **DORSEY & WHITNEY LLP.**

☐ Check Enclosed.

Extra Claim Fees

Current Claims		Prior		Extra		Fee		Fee Paid
Total	52	- 52	=	0	x	$ 50	=	$ 0
Ind.	8	- 8	=	0	x	$ 200	=	$ 0
Multiple Dependent Claims					x	$	=	$
				Subtotal (Extra Claims)				$ 0

Petition Fee Under 37 CFR 1.17(f), (g), & (h)

Enclosed is a Petition filed under 37 CFR as indicated below:

☐ Petition Fee under 37 CFR 1.17(f) **Fee $400**

§ 1.53(e)	to accord a filing date.
§ 1.57(a)	to accord a filing date.
§ 1.182	for decision on a question not provided for.
§ 1.183	to suspend the rules.
§ 1.378(e)	for reconsideration of decision on petition refusing delayed payment of maintenance fee in expired patent.
§ 1.174(b)	to accord a filing date to an application under §1.740 for extension of patent term.

☐ Petition Fee under 37 CFR 1.17(g) **Fee $200**

§ 1.12	**for access to an assignment record.**
§ 1.14	**for access to an application.**
§ 1.47	**for filing by other than all inventors or person not the inventor.**
§ 1.59	**for expungement of information.**
§ 1.103(a)	**to suspend action in an application.**
§ 1.136(b)	**for review of a request for ext. of time when** §1.136(a) not avail.
§ 1.295	for review of refusal to publish a statutory invention registration.
§ 1.296	to withdraw a req. for pub. after notice of intent to publish issued.
§ 1.377	for review of decision refusing to accept a maintenance fee filed prior to expiration of a patent.
§ 1.550(c)	**for request for ext. of time in** *ex parte* reexam. proceedings.
§ 1.956	**for request for ext. of time in** *ex parte* reexam. proceedings.
§ 5.12	for expedited handling of foreign filing license.
§ 5.15	for changing the scope of a license.
§ 1.5.25	for retroactive license.

☐ Petition Fee under 37 CFR 1.17(h) **Fee $130**

§ 1.19(g)	to request documents in a form other than provided in this part.
§ 1.84	for accepting color drawings or photographs.
§ 1.91	for entry of a model or exhibit.
§ 1.102(d)	to make an application special.
§ 1.138(c)	to expressly abandon an application to avoid publication.
§ 1.313	to withdraw an application from issue.
§ 1.314	to defer issuance of a patent.

FEE CALCULATION (Continued)

3. ADDITIONAL FEES

Large Entity Fee	Small Entity Fee	Fee Description	Fee paid
50	25	Surcharge - late provisional filing fee or cover sheet	$
130	65	Surcharge – Late nonprovisional filing fee or oath	$
180	180	Submission of IDS	$
40	40	Recording each patent assignment per property (times number of properties)	$
120	60	Extension for reply within first month	$
450	225	Extension for reply within second month	$
1,020	510	Extension for reply within third month	$
1,590	795	Extension for reply within fourth month	$
2,160	1,080	Extension for reply within fifth month	$
790	395	Submission After Final 1.129	$
500	250	Notice of Appeal	$
500	250	Filing a brief in support of an appeal	$
1,000	500	Request for oral hearing	$
130	65	Terminal Disclaimer Fee	$
800	400	Design Issue Fee	$
790	395	Request for Continued Examination (RCE)	$
130		Request for voluntary publication or republication	$
500	250	Petition to Revive – unavoidable	$
1,500	750	Petition to Revive – unintentional	$
200		Filing for patent term adjustment	$
400		Request for reinstatement of term reduced	$
1,120		Extension of term of patent	$
OTHER FEE (specify)			$
		Subtotal (Additional Fees)	$0
		Total Amount of Payment:	**$0**

Submitted by:

CUSTOMER NUMBER	DORSEY & WHITNEY LLP	1420 Fifth Avenue, Suite 3400 Seattle, WA 98101-4010 (206) 903-8800 *phone* / (206) 903-8820 *fax*
27,076		

Name: Edward W. Bulchis	Reg. No.: 26,847
Signature: Edward W. Bulchis	Date: 1/6/06